



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/720,162

11/25/2003

Atsushi Kuwata

8001-1176

4322

466

7590

08/15/2006

YOUNG & THOMPSON  
745 SOUTH 23RD STREET  
2ND FLOOR  
ARLINGTON, VA 22202

EXAMINER

SUN, SCOTT C

ART UNIT

PAPER NUMBER

2182

DATE MAILED: 08/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/720,162

Applicant(s)

KUWATA, ATSUSHI

Examiner

Scott Sun

Art Unit

2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 30 May 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 May 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/30/2006 has been entered.

### ***Response to Arguments***

2. Applicant's arguments in the remarks are summarized as:
- a. Prior art of record does not teach the new claim limitation "substantially simultaneously writing data and check information to first and second disks".
3. Regarding argument 'a', applicant argues that Rivard teaches each WCC operates autonomously with respect to each other WCC (paragraph 49) and therefore cannot write substantially simultaneous to first and second disks. Examiner notes Rivard teaches that "each WCC can operate autonomously" (emphasis added), and that doing so would provide "a fully redundant system, there is no single point of failure that can cause an interruption of service". This does not imply the WCC modules cannot synchronize with each other and execute commands simultaneously. Even if the WCC

Art Unit: 2182

modules only operate autonomously, this would provide more motivation (e.g. speed up processing) to write to the disks simultaneously because the WCC modules operate in parallel.

Applicant further argues that Weber teaches separating DRIVE B (data drive) and DRIVE A (parity drive) read and write operations and therefore does not teach substantially simultaneously. Although examiner agrees that Weber teaches an early write method (write data before parity) for performance reasons, Weber also acknowledges there are tradeoffs to such techniques because additional hardware are needed (battery, power failure logic; column 3, lines 1-25, 50-70; column 4, lines 1-20). Therefore, Weber does not teach away from substantially simultaneous writing data and parity. Instead, Weber merely teaches an alternative way that can be used to improve performance with the tradeoff of increased cost.

Lastly, even assuming neither Rivard nor Weber teach explicitly "substantially simultaneous writing data and parity to the first and second disks", examiner notes that such teachings are also missing in applicant's own disclosure (see U.S.C. 112 rejections below).

4. Having addressed each of applicant's arguments, the following rejections are made in light of the above discussions and in response to applicant's amended claims.

#### ***Claim Rejections - 35 USC § 112***

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the

Art Unit: 2182

art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1-16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Specifically, the disclosure does not recite nor suggest "substantially simultaneously" writing data and parity to first and second disks. Examiner notes that such teachings are missing from both the portions referenced by applicant's remarks ("figure 6, step S28", "page 16, line 12, to page 18, line 1, and page 19, line 23 to page 20, line 9") and the remainder of the disclosure. In fact, the disclosure states "it is an object of the present invention to provide a disk array apparatus which maintains data coherency in a case wherein, when the write data and check information are being written to a data disk for storing the write data and a check information disk for storing the check information, respectively, one of the data and the check information can be written, but the other cannot be written". This contradicts the claimed invention in which the data and the check information are written simultaneously.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Regarding claims 1, 7, and 11, the limitation "substantially simultaneously" renders the claim scope indefinite. The term "substantially" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

10. The following rejections are made based on the examiner's best interpretation of the claims in light of the 35 USC 112 rejections above.

***Claim Rejections - 35 USC § 103***

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rivard (PG Pub# US2004/0078508 A1) in view of Weber (US Patent #5,596,708).

13. As per claim 1, Rivard discloses a disk array apparatus (figure 2) comprising a cache memory (data store 210) that temporarily stores data to be read from or written to first and second disks (paragraphs 45, 48, 54-56); Examiner notes that Rivard teaches

Art Unit: 2182

data store 210 holds read data, and WCC, which functions as a write cache and controller, can be integrated with the data store. Alternatively, WCC can be implemented to also have a read cache (paragraph 56).

Rivard further teaches a control unit (cache access concentrator 201, comprising WCC units) which transforms said data into a physical domain of said cache memory so as to associate said data with physical addresses and processes for preferentially writing the data associated with the physical addresses in the cache memory to the first and second disks (paragraphs 55, 58; 70); Examiner notes that Rivard teaches WCC uses a protocol such as SCSI or ATAPI for communication with the disks, in either case LBA (logical block address) of the data would be used. In order to read or write data to the physical disk, LBA is translated (transformed) into a corresponding physical disk block location, usually in terms of cylinder-head-sector. It would then allow the data to be written to the physical disks.

Although Rivard teaches write scheduling and a plurality of disks, Rivard does not teach explicitly generating check information, and writing the data and check information substantially simultaneously to first and second disks. However, Weber teaches a first disk (drive a) and a second disk (drive b; figure 5), and wherein a control unit processes substantially simultaneously said data and said check information to said first and second disks (column 8, lines 9-51). Examiner notes that Weber teaches data may be stored before parity data in the event that parity drive is unavailable, which suggests that when both drives are available, both data and parity are stored substantially simultaneous. This is also analogous to the teachings of application's

vet 8/10/16  
as best understood in light of the prior art

disclosure (page 3, lines 8-14). Teachings of Rivard and Weber are from the same field of disk storage systems, and specifically of read/write performance.

Therefore, it would have been obvious at the time of invention for a person of ordinary skill in the art to combine teachings of Rivard and Weber by using the scheduling technique of data and parity data disclosed by Weber in the storage system of Rivard for the benefit of efficient utilization of the disk drives (Weber; column 8, lines 42-44).

14. As per claim 2, Rivard and Weber combined discloses the disk array apparatus as claimed in claim 1, and Rivard further teaches wherein said control unit releases the data associated with the physical addresses in the cache memory from a state in which the data is associated with the physical addresses after confirming that the writing is completed (paragraph 69).

15. As per claim 3, Rivard and Weber combined discloses the disk array apparatus as claimed in claim 1, and Rivard further teaches wherein said control unit comprises a plurality of control units (write cache controllers) which are physically independent of one another and wherein if a failure occurs in one control unit, another control unit takes over the preferential processing for the data associated with a physical address in the cache memory (paragraph 81).

16. As per claims 4-6, Rivard and Weber combined discloses the disk array apparatus as claimed in claim 1-3, wherein Rivard further teaches wherein said cache memory is a nonvolatile memory (paragraph 51, 52, 81). Examiner notes Rivard also teaches the use of NVRAM (non-volatile RAM) in prior art systems (paragraph 26).



17. As per claims 7-16, the examiner finds these claims contain substantially similar limitations as above rejected claims 1-6. Therefore, the same arguments are applied.

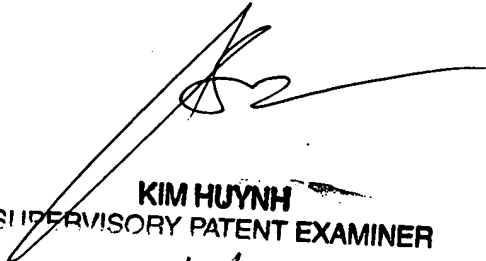
**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Sun whose telephone number is (571) 272-2675. The examiner can normally be reached on M-F, 10:30am-7pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

  
**KIM HUYNH**  
SUPERVISORY PATENT EXAMINER  
8/10/02